UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/407,204	09/28/1999	MING-TUNG SHEN	8688.128US01	2434

23552 7590 07/25/2002

MERCHANT & GOULD PC
P.O. BOX 2903
MINNEAPOLIS, MN 55402-0903

EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	18

DATE MAILED: 07/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/407,204	Shen
Examiner	**Art Unit**
Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 16, 2002*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-6 and 19-21* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-6 and 19-21* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 6, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al (US Pat. 6051878) in view of Bertin et al (US Pat. 5977640), Panchou et al (US Pat. 6040630) and Clayton (US Pat. 5731633).

Regarding claim 1, Akram et al disclose a semiconductor stacked device/multichip module(MCM) comprising:

- a chip mounting member/printed circuit board-PCB (140/116 in Fig. 1; Col. 4, line 50) having opposite first and second surfaces, a set of circuit traces (not numerically referenced in Fig. 1) and a plurality of conventional vias/traces (158/136 in Fig. 1) that extend in/on the first and second surfaces and are connected to the circuit traces

- a first and second semiconductor chips (162/150 in Fig. 1) on top and bottom surfaces of the PCB respectively and the semiconductor chips having a pad mounting surface with a plurality of contact pads/terminals (166 in Fig. 1) provided thereon
- a first and second conductor units including a plurality of conventional conductive contact bumps (144 in Fig. 1) and wire bond terminals (not numerically referenced in Fig. 1) respectively for electrically connecting the contact pads of the semiconductor chips and respective circuit traces
- the first or second semiconductor chips being bonded by a conventional methods comprising flip chip bonding/conductive adhesive/tape, TAB tape/dielectric tape, wire bonding, etc. (Col. 3, line 63), and
- plurality of solder balls/external connections (148 in Fig. 1; Col. 3, line 55) disposed on one or both surfaces of the chip mounting member

(Fig. 1; Fig. 1-6; Col. 3-10).

Akram et al disclose the conventional vias/traces (158/136 in Fig. 1) providing the electrical connections through the substrate but fail to specify them being plated through holes.

It is conventional in the chip packaging and interconnection technology art to use vias/traces/through-holes being conductive/plated through-holes to provide the electrical connection between the surfaces/layers of the substrate. Bertin et al teach

using a wiring in a variety of conventional configurations such as conductive traces, through-holes, channels, etc. (25 in Fig. 3, 7, 16, etc.) to provide an electrical connection through/within the substrate with respectively aligned solder balls. The cited reference by Londa teaches using such conventional through-holes connecting the circuit traces between the top and bottom surfaces of the substrate being plated through-holes and further using respectively aligned solder balls (42, 44, 66, 68, etc. in Fig. ½; Col. 4) to provide an interconnection between the substrates.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the wiring/through-hole traces being plated through holes so that the desired electrical/external connections can be achieved using Bertin et al's substrate structure in Akram et al's chip module.

Regarding claim 2, Akram et al disclose the first semiconductor chip being conventionally bonded to the chip mounting member/PCB using flip chip bonding/conductive adhesive/tape but fail to specify using a first dielectric tape for bonding/securing adhesively with the a plurality of holes at positions registered with the first conductor unit including a plurality contact pads/balls of the first semiconductor chip to bond and establish the electrical connection between the chip to the first circuit traces on the chip mounting member/substrate and aligning/connecting solder balls to the respective plated through holes.

Panchou et al teach using a conventional attachment film/dielectric tape with a plurality of holes at positions in registration with the corresponding contact pads/balls of the chip in adhesive bonding of a flip chip device (Fig. 4 and 4a; Col. 5; Fig. 1-4).

Clayton teaches using the conventional adhesive film/dielectric tape for bonding the first and second semiconductor chips on the circuit substrate (Fig. 18A-D; Col.. 11, line 36; Col. 18, line 50) in a multichip module with wire bonding (Fig. 18C) or flip chip bonding (Fig. 18D). Clayton further teaches disposing the first circuit traces and the first semiconductor chip on the same surface of the chip mounting member/substrate and forming the bonding with the contact pads/balls being registered with those of the chip and the substrate (74 and 76 in Fig. 18D; Col. 19, line 33) in flip chip.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to use a first dielectric tape for bonding/securing adhesively with a plurality of holes at positions registered with the first conductor unit including a plurality contact pads/balls of the first semiconductor chip to bond and establish the electrical connection between the chip to the first circuit traces on the chip mounting member/substrate so that chip bonding can be improved using Panchou et al, Clayton and Bertin et al's bonding structures in Akram et al.

Regarding claims 3, 4, 20 and 21, the claim elements have been addressed in the rejections as explained above for claims 1 and 2.

Regarding claim 6, Akram et al fail to specify securing a heat dissipating plate on the heat dissipating surface opposite to the pad mounting surface of the chip.

Bertin et al teach using conventional heat spreader/plate secured on the heat dissipating surface opposite to the pad mounting surface of the chip (Fig. 7 and 15; Col. 4, line 16) to improve heat dissipation.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a heat dissipating plate on the heat dissipating surface opposite to the pad mounting surface of the chip so that heat dissipation can be improved using Bertin et al, Panchou et al and Clayton's structures in Akram et al's module.

3. Claims 5 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al (US Pat. 6051878) in view of Bertin et al (US Pat. 5977640), Panchou et al (US Pat. 6040630), Clayton (US Pat. 5731633) and further in view of Tanioka (US Pat. 5784264) and Londa (US Pat. 6101100).

Regarding claim 5, as explained above for claims 1-4, Akram et al disclose providing a polymer resin/epoxy (168 in Fig. 1; Col. 6, line 60) on the bottom peripheral portion to strengthen the bonding of the first semiconductor chip with the same one of the surfaces of the chip mounting member/PCB but fails to specify using resin on the peripheral side portion of the chip.

Tanioka (Fig. 6A) and a cited reference by Egawa (resin 22 in Fig. 2; Col. 4) teach using conventional epoxy/resin on the peripheral/side portion to strengthen the bonding of the first semiconductor chip.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to provide an epoxy resin on the peripheral side portion of the chip so that the bonding of the first semiconductor chip with the chip mounting member/PCB can be improved using Tanioka and Egawa's resin structures in Akram et al in view of Bertin et al, Panchou et al and Clayton.

Regarding claim 19, as explained above for claims 1-4, Akram et al teach using conventional stacking of two identical semiconductor chip modules using alignment of respective external pin or solder ball connections with traces/through-holes (148/136/126 in Fig.1; Col. 4, line 36-57) of upper and lower modules to form a multiple stack.

Londa teaches using the solder balls/bumps aligned to the respective plated through holes extending through upper and lower surfaces of each module and connecting the two modules (10 and 10' in Fig. 2) to form a stacked semiconductor chip module comprising upper and lower semiconductor chip (Col. 4).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a stack comprising upper and lower semiconductor chip modules such that the solder balls/bumps aligned to the respective plated through holes of each module so that a multi-level connection capability can be achieved using Londa's stack layout Akram et al's MCM in view of Bertin et al, Panchou et al, Clayton (US Pat. 5731633) and Tanioka.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

07-19-02

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800